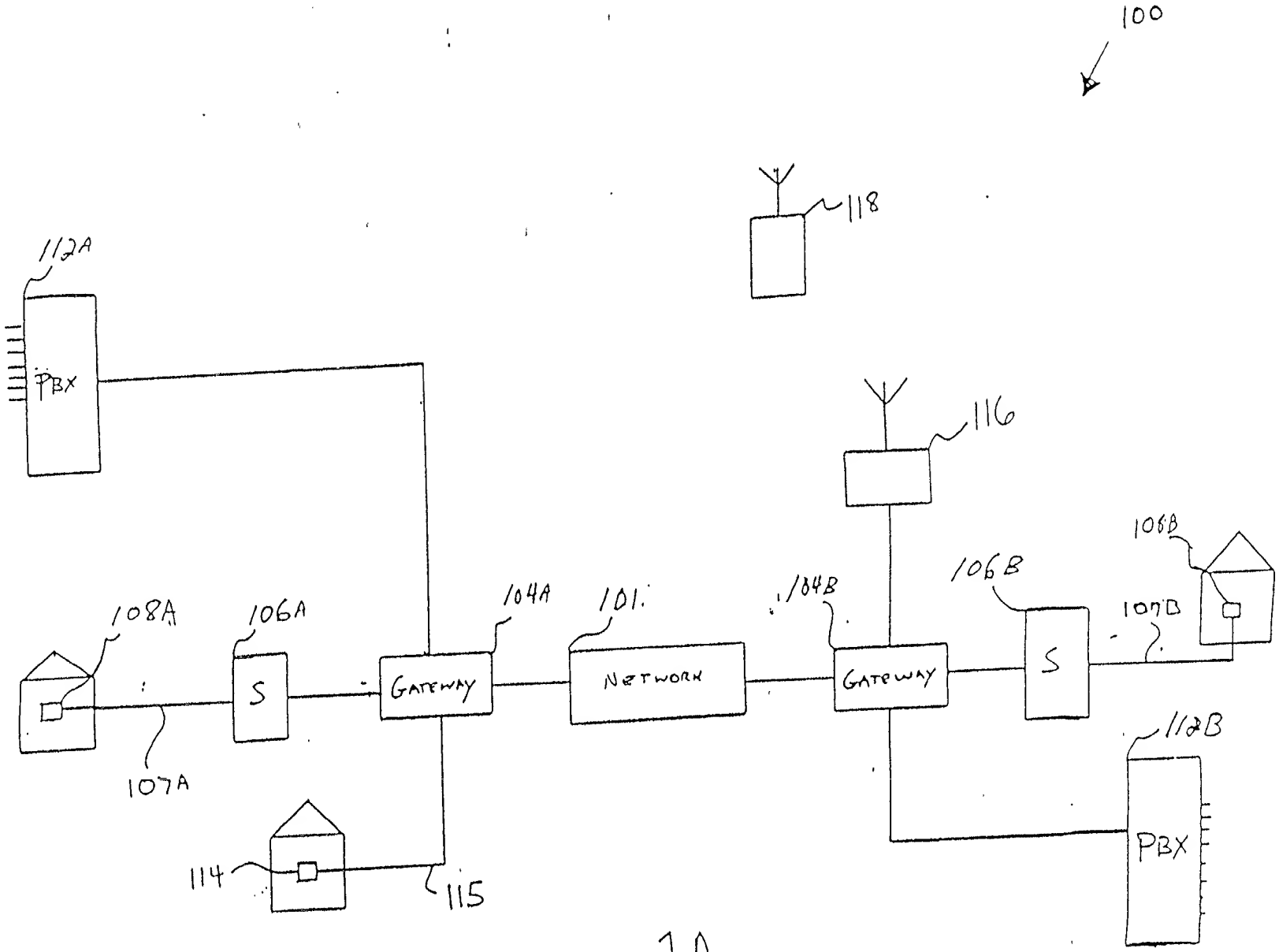
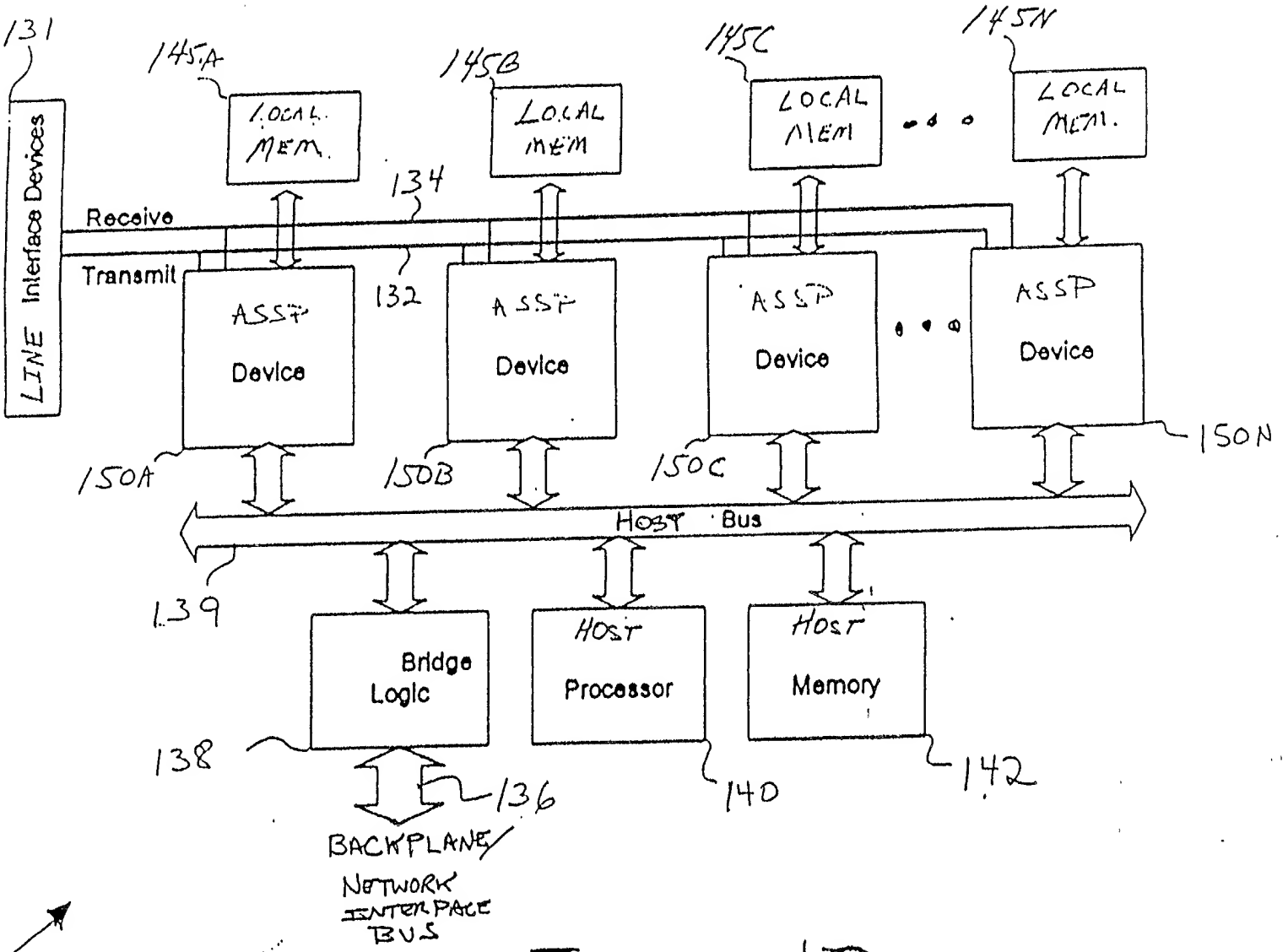

100
118
112A
PBX
116
106B
108B
108A
106A
104A
101
104B
106B
107B
S
GATEWAY
NETWORK
GATEWAY
S
107A
112B
114
115
PBX

FIG. 1A


131
LINE Interface Devices
145A
LOCAL MEM.
145B
LOCAL MEM
145C
LOCAL MEM
145N
LOCAL MEM.
134
Receive
Transmit
132
ASSP Device
ASSP Device
ASSP Device
ASSP Device
150A
150B
150C
150N
Host Bus
139
Bridge Logic
Host Processor
Host Memory
138
136
140
142
BACKPLANE / NETWORK INTERFACE BUS

130

FIG. 1B

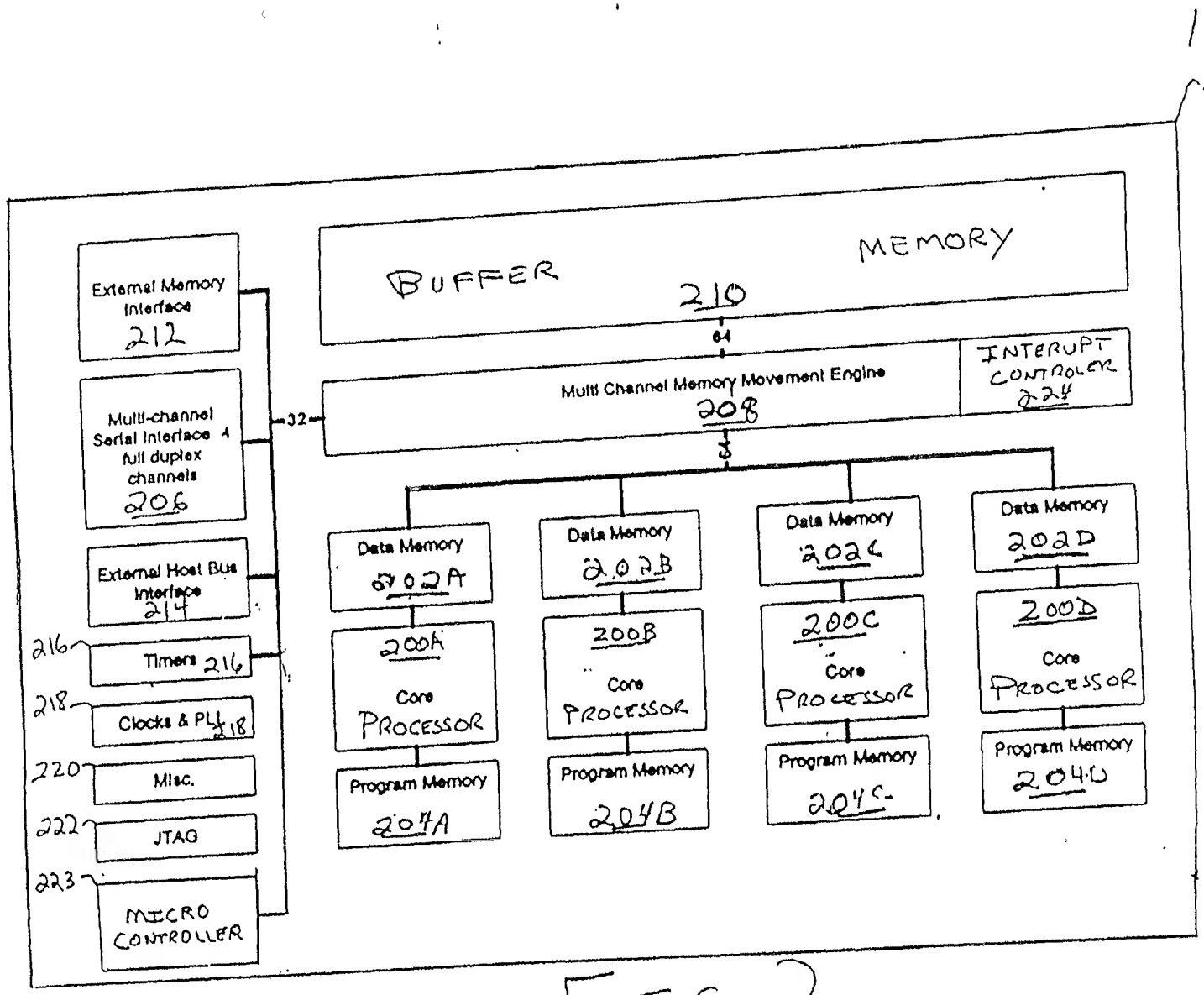

150
BUFFER MEMORY
210
64
Multi Channel Memory Movement Engine
208
INTERUPT CONTROLLER
224
32
64
External Memory Interface
212
Multi-channel Serial Interface 4 full duplex channels
206
External Host Bus Interface
214
216
Timers 216
218
Clocks & PLL 218
220
Misc.
222
JTAG
223
MICRO CONTROLLER
Data Memory
202A
200A
Core
PROCESSOR
Program Memory
204A
Data Memory
202B
200B
Core
PROCESSOR
Program Memory
204B
Data Memory
202C
200C
Core
PROCESSOR
Program Memory
204C
Data Memory
202D
200D
Core
PROCESSOR
Program Memory
204D

FIG. 2

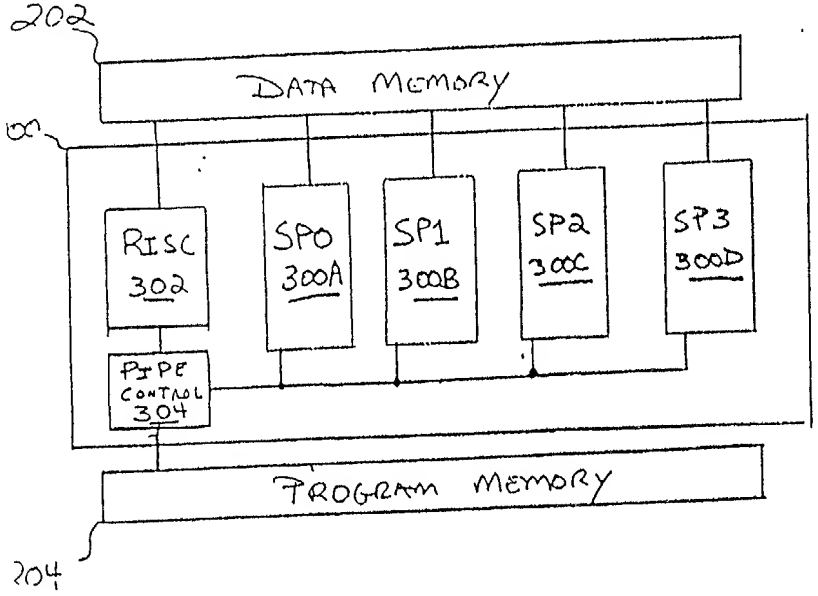


FIG. 3

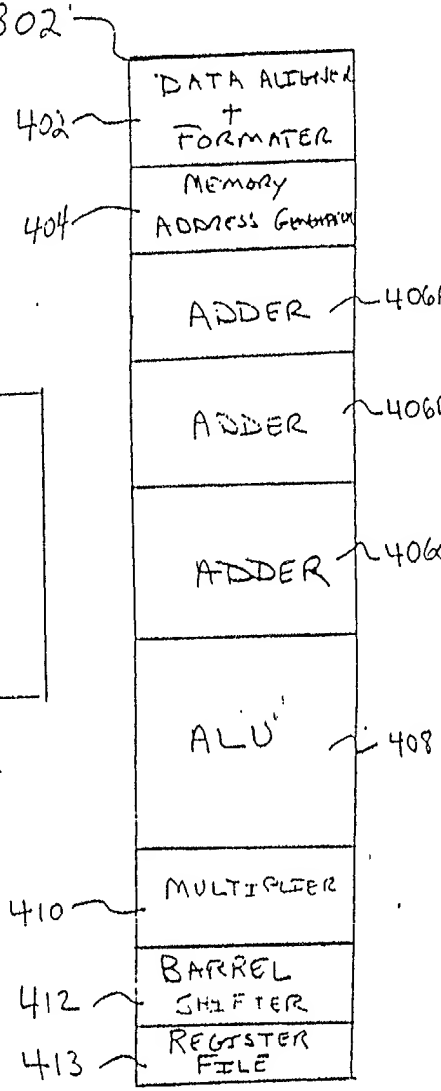


FIG. 4

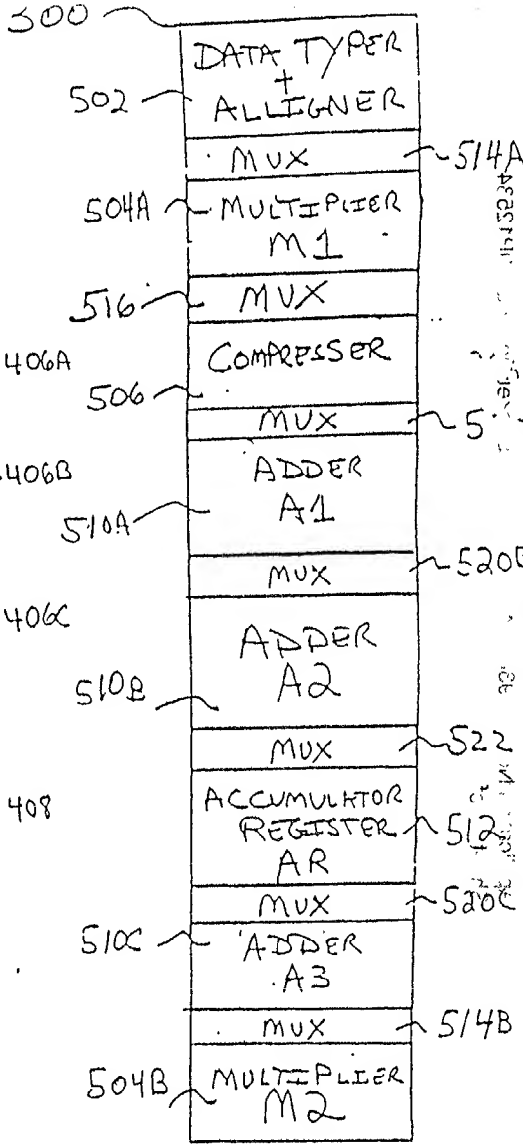


FIG. 5A

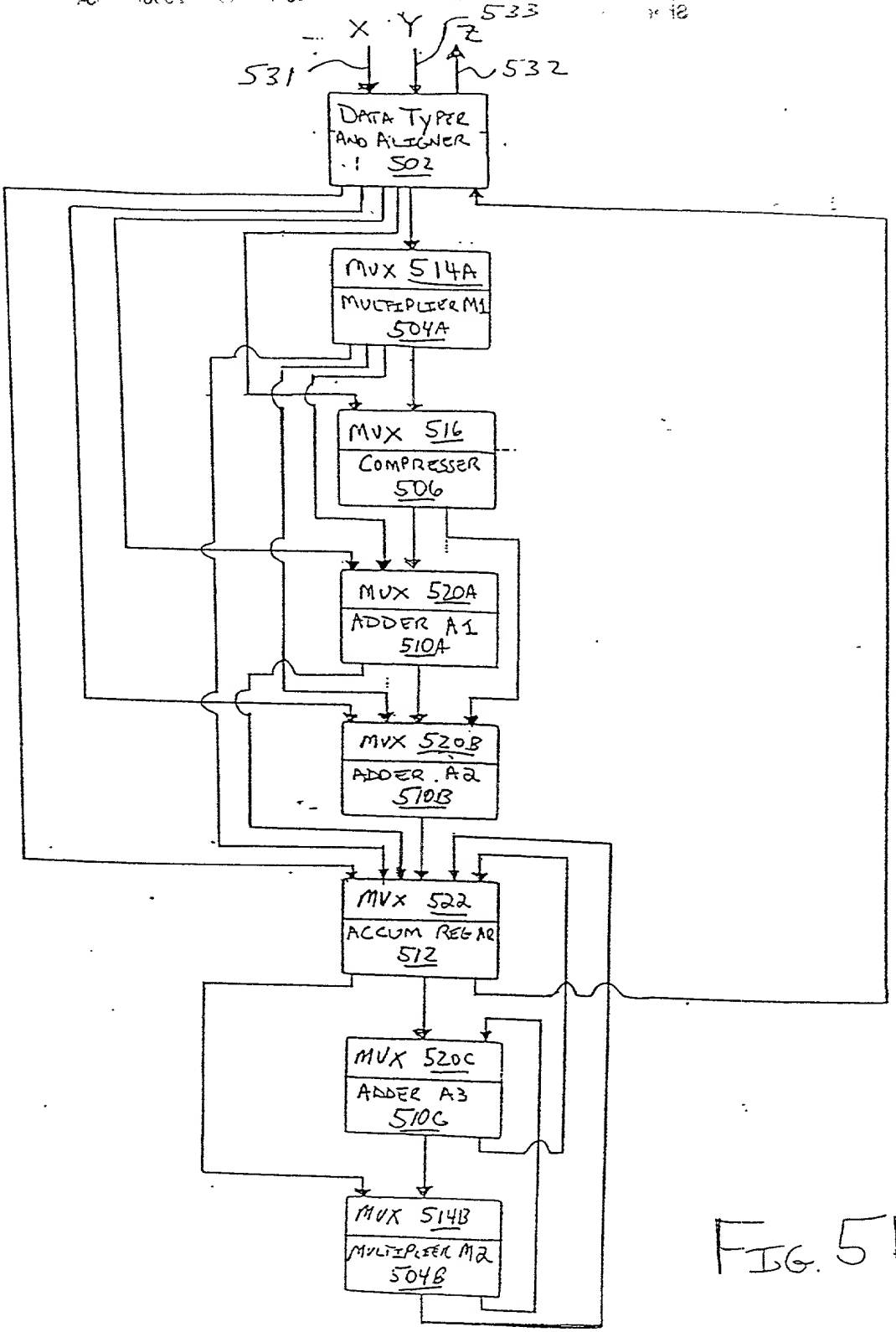

X
Y
Z
533
531
532
DATA TYPER AND ALIGNER 502
MUX 514A
MULTIPLIER M1 504A
MUX 516
COMPRESSER 506
MUX 520A
ADDER A1 510A
MUX 520B
ADDER A2 510B
MUX 522
ACCUM REGAR 512
MUX 520C
ADDER A3 510C
MUX 514B
MULTIPLIER M2 504B

FIG. 5B

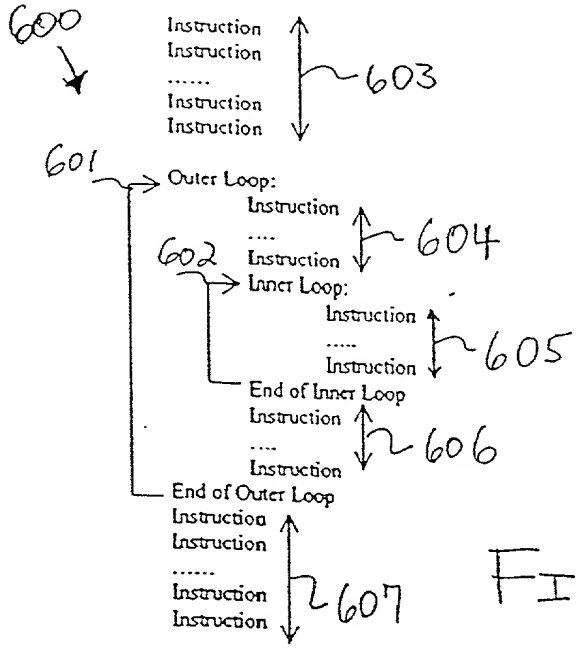


FIG. 6A

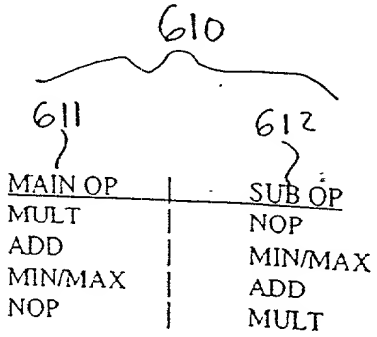


FIG. 6B

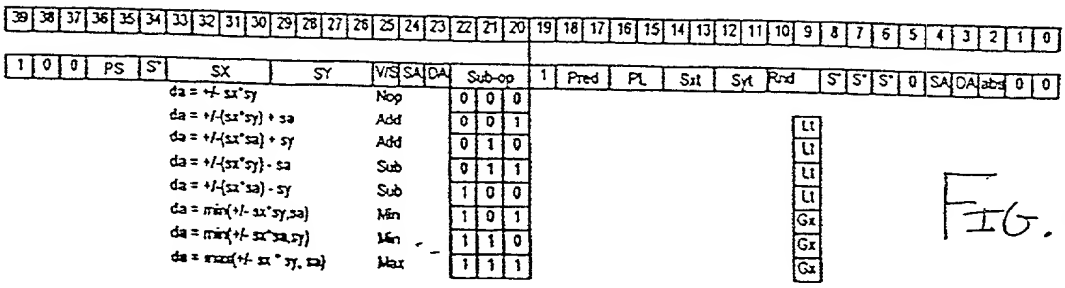


FIG. 6C

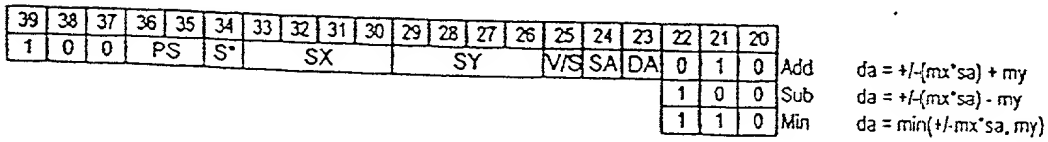


FIG. 6D

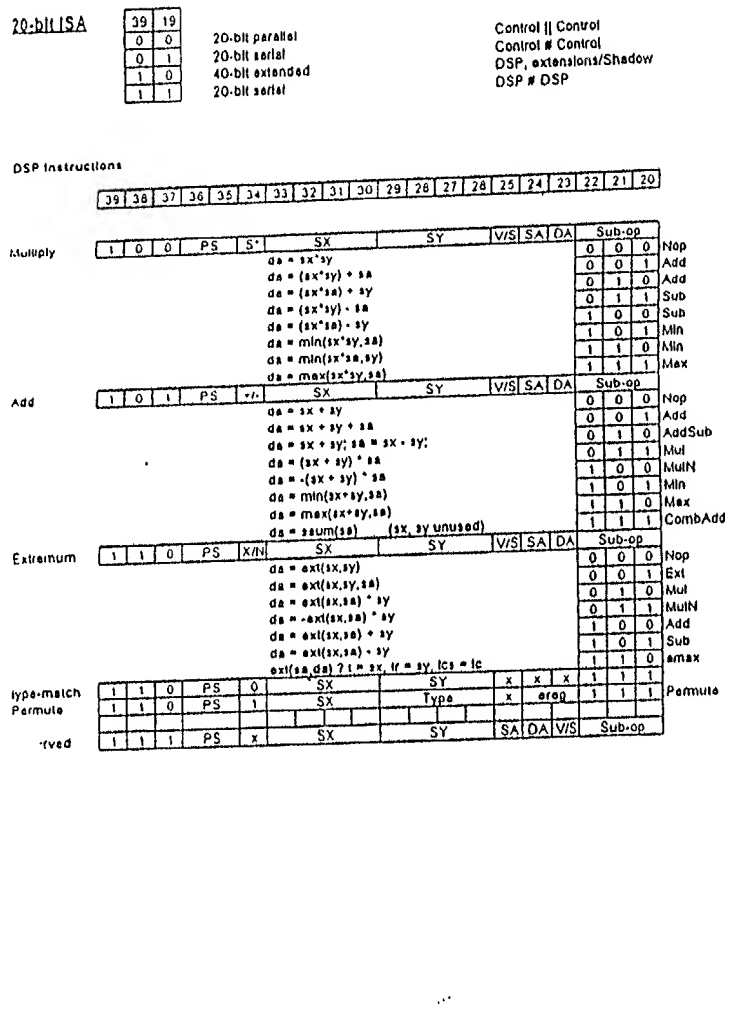

20-bit ISA
39 19
0 0 20-bit parallel
0 1 20-bit serial
1 0 40-bit extended
1 1 20-bit serial
Control || Control
Control # Control
DSP, extensions/Shadow
DSP # DSP
DSP Instructions
39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20
Multiply
1 0 0 PS S* SX SY V/S SA DA Sub-op
da = sx*sy
da = (sx*sy) + sa
da = (sx*sa) + sy
da = (sx*sy) - sa
da = (sx*sa) - sy
da = min(sx*sy,sa)
da = min(sx*sa,sy)
da = max(sx*sy,sa)
0 0 0 Nop
0 0 1 Add
0 1 0 Add
0 1 1 Sub
1 0 0 Sub
1 0 1 Min
1 1 0 Min
1 1 1 Max
Add
1 0 1 PS +/- SX SY V/S SA DA Sub-op
da = sx + sy
da = sx + sy + sa
da = sx + sy; sa = sx - sy;
da = (sx + sy) * sa
da = -(sx + sy) * sa
da = min(sx+sy,sa)
da = max(sx+sy,sa)
da = asum(sa) (sx, sy unused)
0 0 0 Nop
0 0 1 Add
0 1 0 AddSub
0 1 1 Mul
1 0 0 MulN
1 0 1 Min
1 1 0 Max
1 1 1 CombAdd
Extremum
1 1 0 PS X/N SX SY V/S SA DA Sub-op
da = ext(sx,sy)
da = ext(sx,sy,sa)
da = ext(sx,sa) * sy
da = -ext(sx,sa) * sy
da = ext(sx,sa) + sy
da = ext(sx,sa) - sy
ext(sa,da) ? i = sx, ir = sy, ics = ic
0 0 0 Nop
0 0 1 Ext
0 1 0 Mul
0 1 1 MulN
1 0 0 Add
1 0 1 Sub
1 1 0 amax
Type-match Permute
1 1 0 PS 0 SX SY x x x 1 1 1 Permute
1 1 0 PS 1 SX Type x areg
rved
1 1 1 PS x SX SY SA DA V/S Sub-op
Control and specifier Extensions
19 18 17 16 15 14 13 12 11 10 0 8 7 6 5 4 3 2 1 0
Mul
0 Pred PL Sxt Syt Rnd LI Gx S* S* S* 0 SA DA adst 0 0
Add/Sub min/max
Add
0 Pred PL Sxt Syt LI Sub-ext 0 SA DA adst 0 0
+/- +/- +/- x
x V/S Rnd Fp
Ir-ctl Gx Fp
Nop (use Mul/MulN Min/max)
Ext
0 Pred PL Sxt Syt Ir-ctl Gx Sub-ext LI Fp Rnd V/S 0 SA DA adst 0 0
Add/sub Mul
0 Pred PL Sxt Pctl 0 areg Pctl 0 0
Type/offset/permute extensions
19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0 Pred PL x Type:SX Type SY 0 SA DA x 0 1
0 Pred PL Pex Permute:SX Permute SY 0 SA DA Pst 1 0
0 Pred I/R I/R p/x Offset SX Offset:SY 0 SA DA pst 1 1
Type override
permute override
Offset override
Shadow DSP
19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0 Op PL op areg areg 1 SA DA Sub-op

FIG. 6 E

Control Instructions

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
add,sub	L	Pred	0	0	0	RX					RY				RZ				+/-	0
max,min	L	Pred	0	0	0	RX					RY				RZ				X/N	1
Shift	L	Pred	0	0	1	RX					UI4				RZ				UI1	R/L
Logic	L	Pred	0	1	0	RX					RY				RZ				&, |	&|
Mux	L	Pred	0	1	1	RX					RY				RZ				Pd	0
mov	L	Pred	0	1	1	RX					DZ				Rxt	Dzt	0	0	0	1
addi	L	Pred	0	1	1	SI4					DZ				x	x	1	0	0	1
mov2srg	L	Pred	0	1	1	RX					unit		sreg		gd	type			1	0	1
Ldm	L	Pred	0	1	1	RX					DZ1				DZ2				1	1
sbits	L	Pred	1	0	0	UI4:POS					RZ				Rzt	UI4				0
bits	L	Pred	1	0	0	UI4:POS					RZ				Rzt	UI2		0	0	1
setbit	L	Pred	1	0	0	UI4:POS					RZ				Rzt	UI1	UI1	1	0	1
Movl	L	Pred	1	0	0	SI8									RZ				-1	1
Jmp	L	Pred	1	0	1	SI9										0	Pred		0	0
Call	L	Pred	1	0	1	SI9										1	Pred		0	0
Loop	L	Pred	1	0	1	UI5 : Lcount					UI5: Lsize							UI2: Lsl	0	1
Jmpi	L	Pred	1	0	1	RX				x	x	x	x	x	0	Pred			1	0
Calli	L	Pred	1	0	1	RX				x	x	x	x	x	1	Pred			1	0
Loopi	L	Pred	1	0	1	RX				x	UI5: Lsize							UI2: Lsl	1	1
Tst	L	Pred	1	1	0	RX					RY				PZ				=, <, >	0
Testbit	L	Pred	1	1	0	RX					UI5				PZ				B	0	1
Andp, orp	L	Pred	1	1	0	Pa			Pb			Pc			PZ				&|	1	1
Load	L	Pred	1	1	1	MX					RZ				Ext				0	0	0
Store	L	Pred	1	1	1	MZ					RX				Ext				1	0	0
aLoad	L	Pred	1	1	1	MX					RZ				1	1	1	0	0	0
aStore	L	Pred	1	1	1	MZ					RX				1	1	1	1	0	0
Extended	L	Pred	1	1	1	Bits 27:16													1	0
Logic2	L	Pred	1	1	1	RX					RY/RZ				Rxt	Ryt	&, |, &|		0	1
mov-srg	L	Pred	1	1	1	unit		sreg			RZ				gd	Sft		0	1	1
Crb	L	Pred	1	1	1	RX					RZ				s/m	0	0	1	1	1
Parity	L	Pred	1	1	1	RX					PZ			O/E	0	1	0	1	1	1
Sim	L	Pred	1	1	1	MZ					RX				1	1	0	1	1	1
Abs	L	Pred	1	1	1	RX					RZ				0	0	1	1	1	1
Neg	L	Pred	1	1	1	RX					RZ				0	1	1	1	1	1
Div-step	L	Pred	1	1	1	RX					RZ				1	0	1	1	1	1
& Set	L	Pred	1	1	1	RX					PZ			0	1	1	1	1	1	1
[illegible]	[illegible]																			
Return	L	Pred	1	1	1	Pred		I-ctl		0	1	0	1	1	1	1	1	1	1	1
Zero-ac	L	Pred	1	1	1	ac #				1	1	0	1	1	1	1	1	1	1	1
aSync	L	Pred	1	1	1	RZ				0	1	1	1	1	1	1	1	1	1	1
Swi	L	Pred	1	1	1	UI3			0	1	1	1	1	1	1	1	1	1	1	1
Nop	L	Pred	1	1	1	UI3			1	1	1	1	1	1	1	1	1	1	1	1

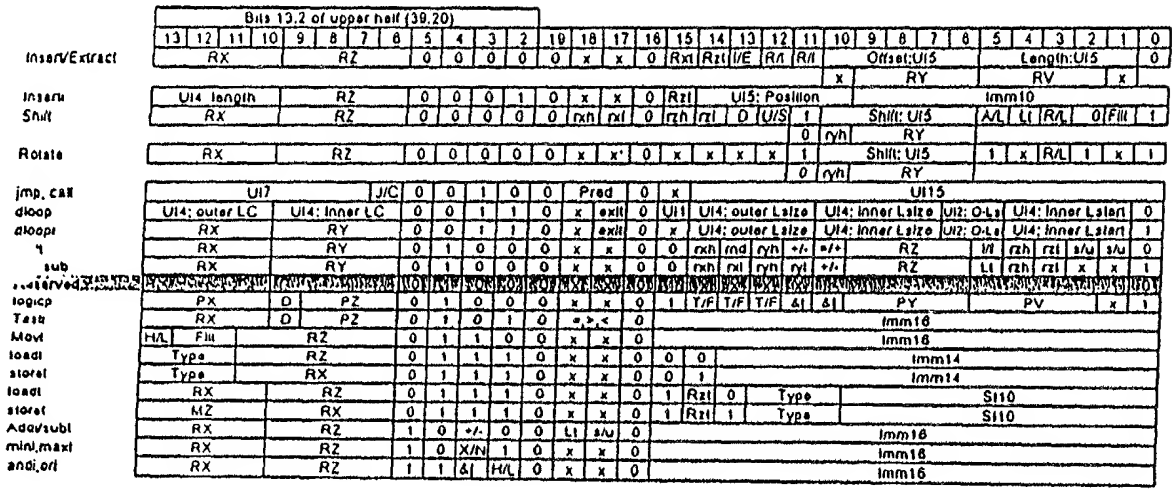
<Bit1, Bits9-6> == UI5 (Shift Amount)

<Bit3, Bits13-10> == UI5 :POS

FIG. 6F

—TOTEZEC bOIBE660

Extended Control



Fill: Sign/Zero

Bit 15 is continuation of Inner LC

andp, orp, andorp, orandp: pz = (px relop py) relop pv

FIG. 6G

Sheet 8 of 8
Apple, Horo & Zarrin LLP

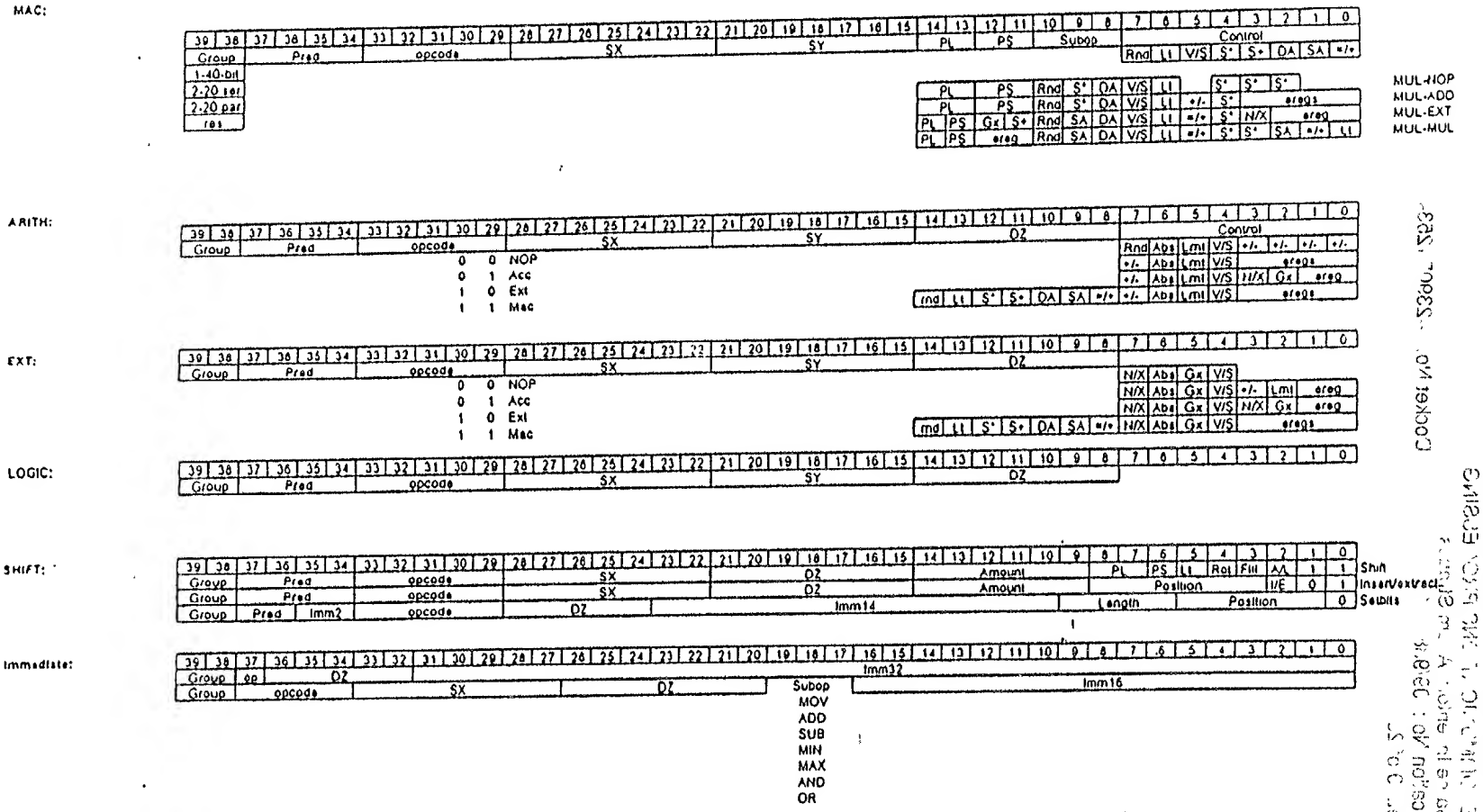

MAC:
ARITH:
EXT:
LOGIC:
SHIFT:
Immediate:
Test:
Branch:
Misc:
Group
Pred
opcode
SX
SY
DZ
Control
Subop
Imm32
Imm16
Imm20
Imm14
Length
Position
Amount
MUL-NOP
MUL-ADD
MUL-EXT
MUL-MUL
NOP
Acc
Ext
Mac
MOV
ADD
SUB
MIN
MAX
AND
OR

FIG. 6H

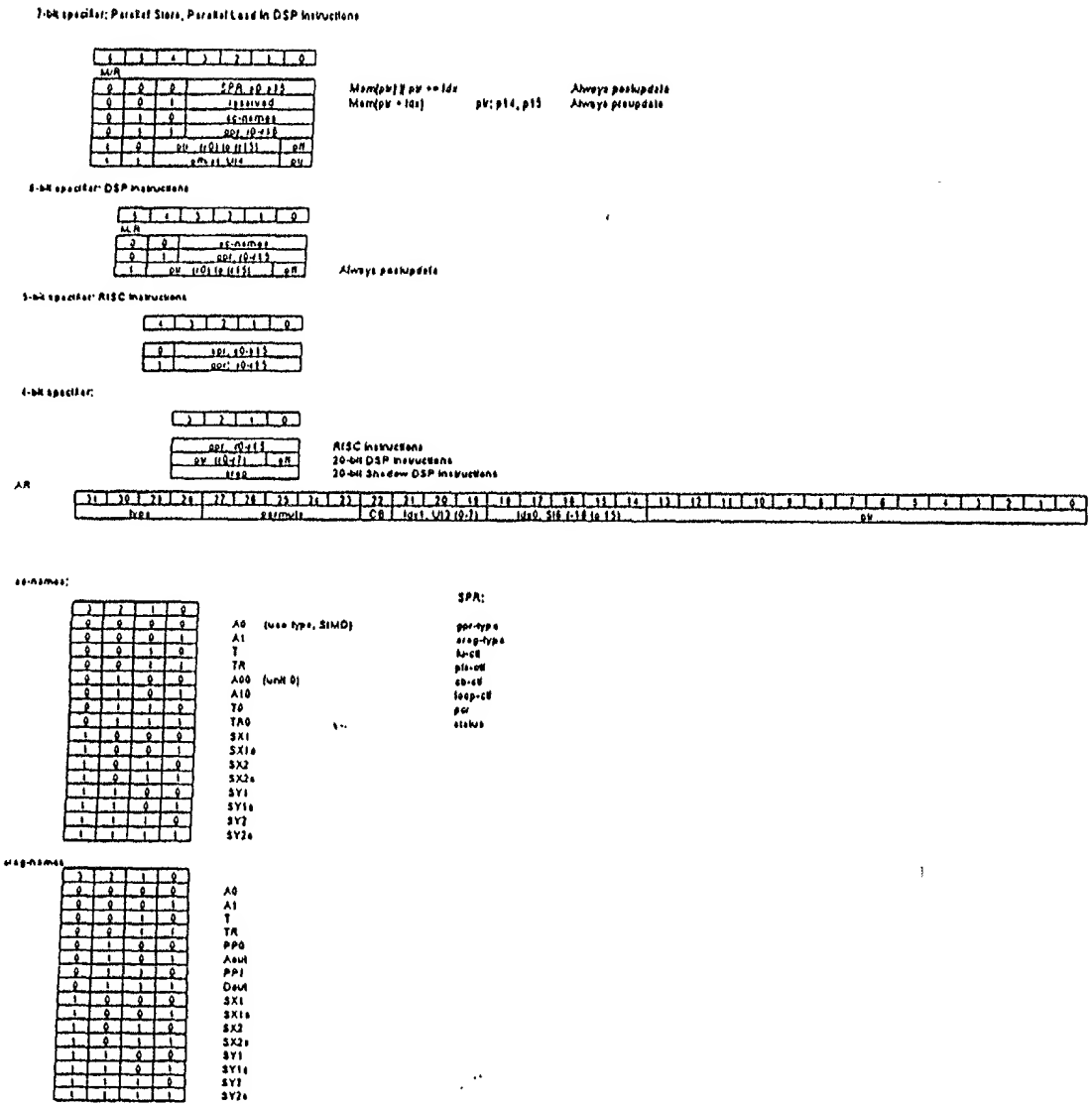

7-bit specifier: Parallel Store, Parallel Load in DSP Instructions
MR
SPA, r0-r15
Mem(pv) || pv += Idx
Mem(pv + Idx)
pv: p14, p15
Always postupdate
Always preupdate
8-bit specifier: DSP instructions
MR
Always postupdate
5-bit specifier: RISC instructions
4-bit specifier:
RISC instructions
20-bit DSP instructions
20-bit Shadow DSP instructions
AR
xx-names:
SPA:
A0 (xxxx type, SIMD)
A1
T
TR
A00 (unit 0)
A10
T0
TR0
SX1
SX1s
SX2
SX2s
SY1
SY1s
SY2
SY2s
per-type
arag-type
ls-ctl
pts-ctl
cb-ctl
loop-ctl
per
status
arag-names:
A0
A1
T
TR
PP0
AouR
PP1
OouR
SX1
SX1s
SX2
SX2s
SY1
SY1s
SY2
SY2s

FIG. 6I

FIG. 7

PD-6201-1050

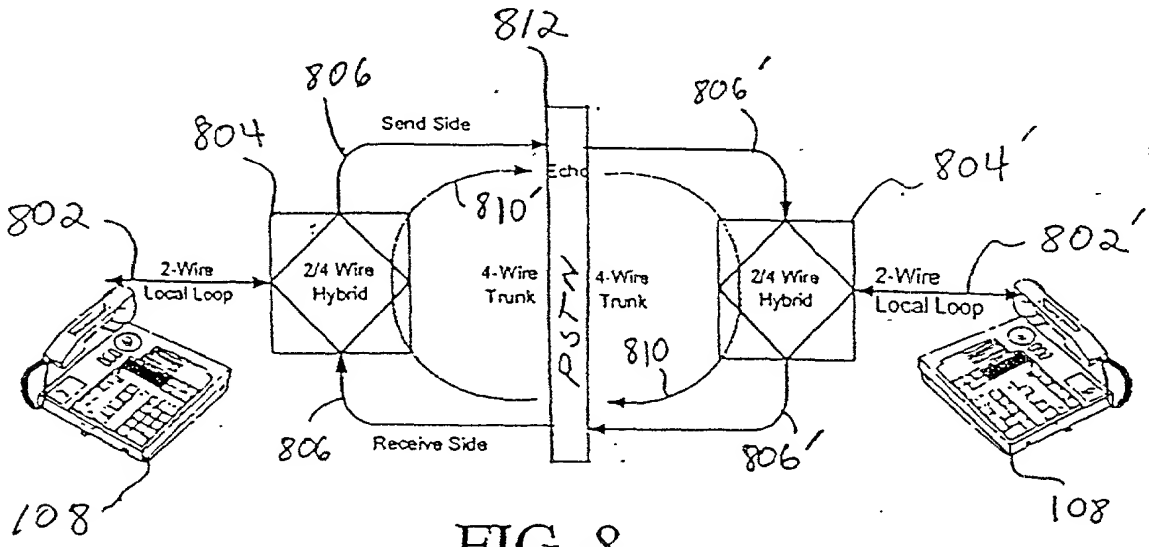


FIG. 8
(PRIOR ART)

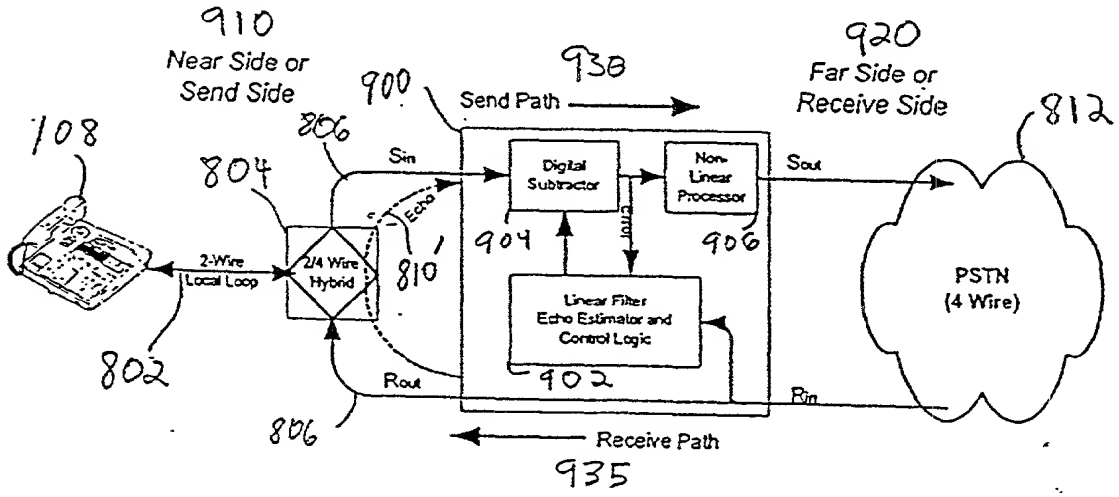


FIG. 9
(PRIOR ART)

FOREST-bOTSE660

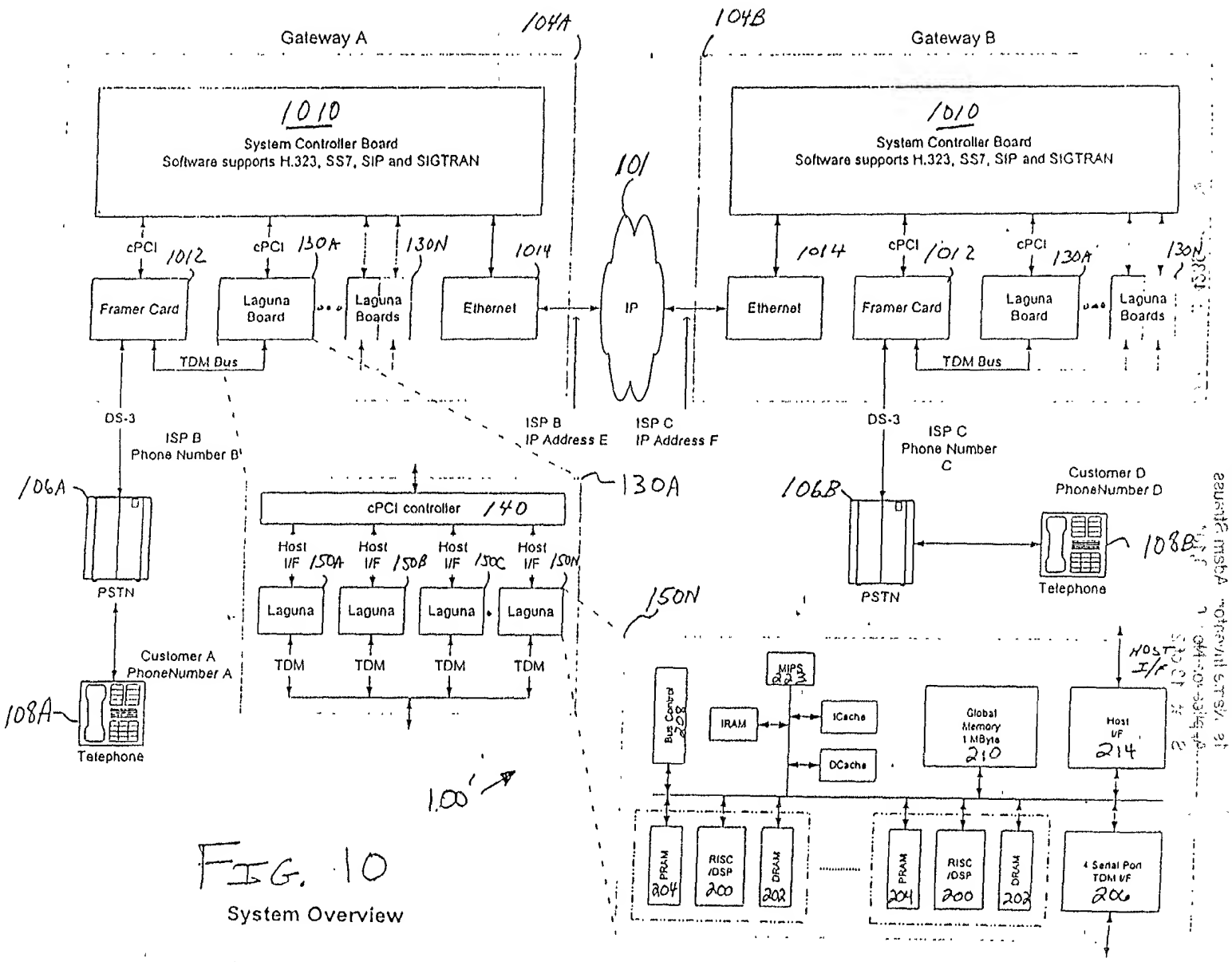


FIG. 10
System Overview

Electronic Publication Information (Rev. 2.0 Jun 2003)
Document Name: US06778660B2.tif
Date and Time: 8/24/2004 10:47:38 AM
Total Pages: 10
Page Number: 5 of 10
Document Type: Drawing
Comments: Application Pages
Sender's Name: Blakely Sokoloff Taylor & Zafman LLP
Fax Number: (714) 557-3800
THIS DOCUMENT MAY BE SCANNED UNDER 37 CFR 1.84(h)(1)
THE COMPLETE ACTIVITY OF THE PROCESS
CHANGE IN DESCRIPTIONS OR CLASSIFICATIONS
OR SUGGESTIONS PRODUCED BY THE

Patent Application Publication

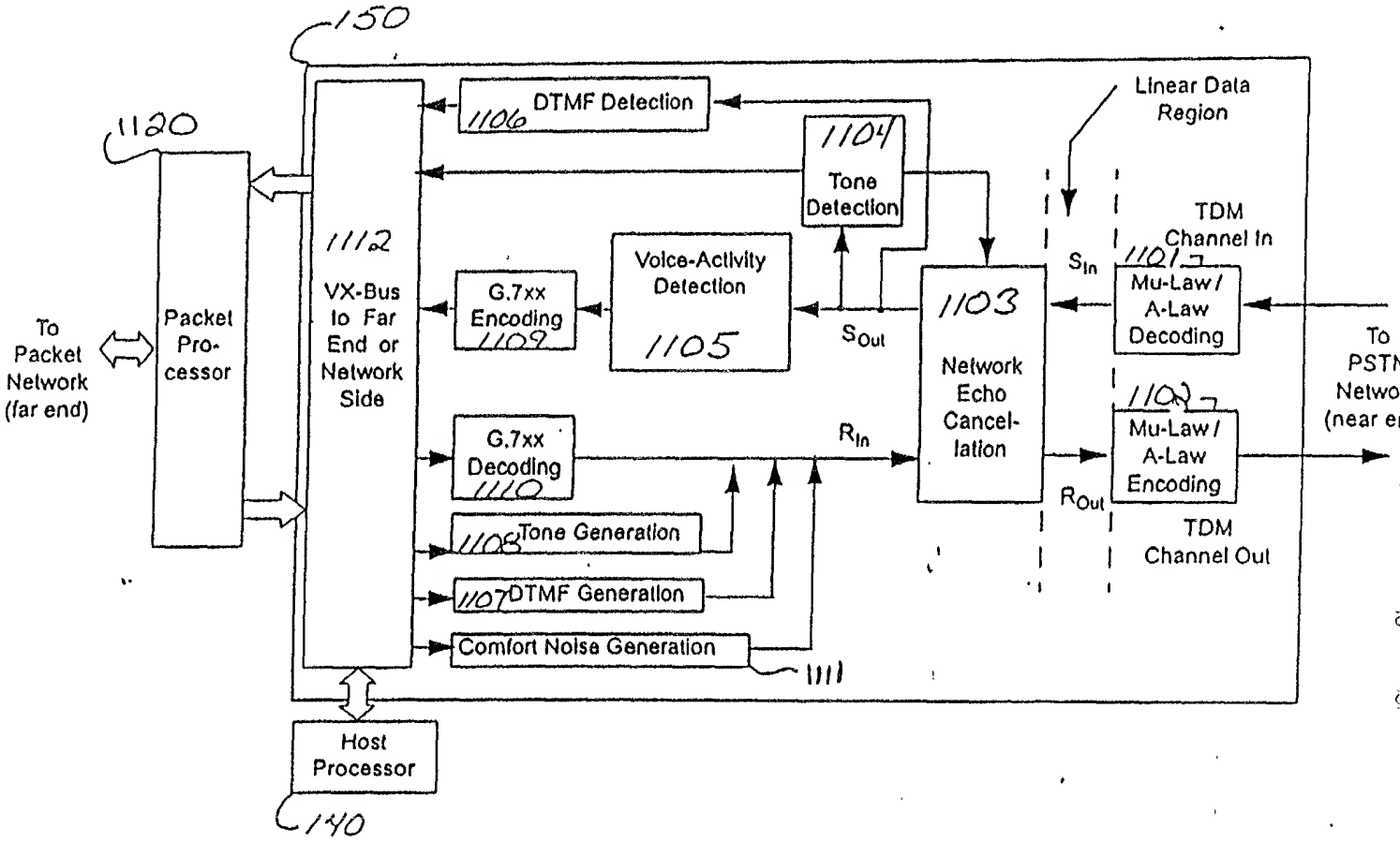


FIG. 11

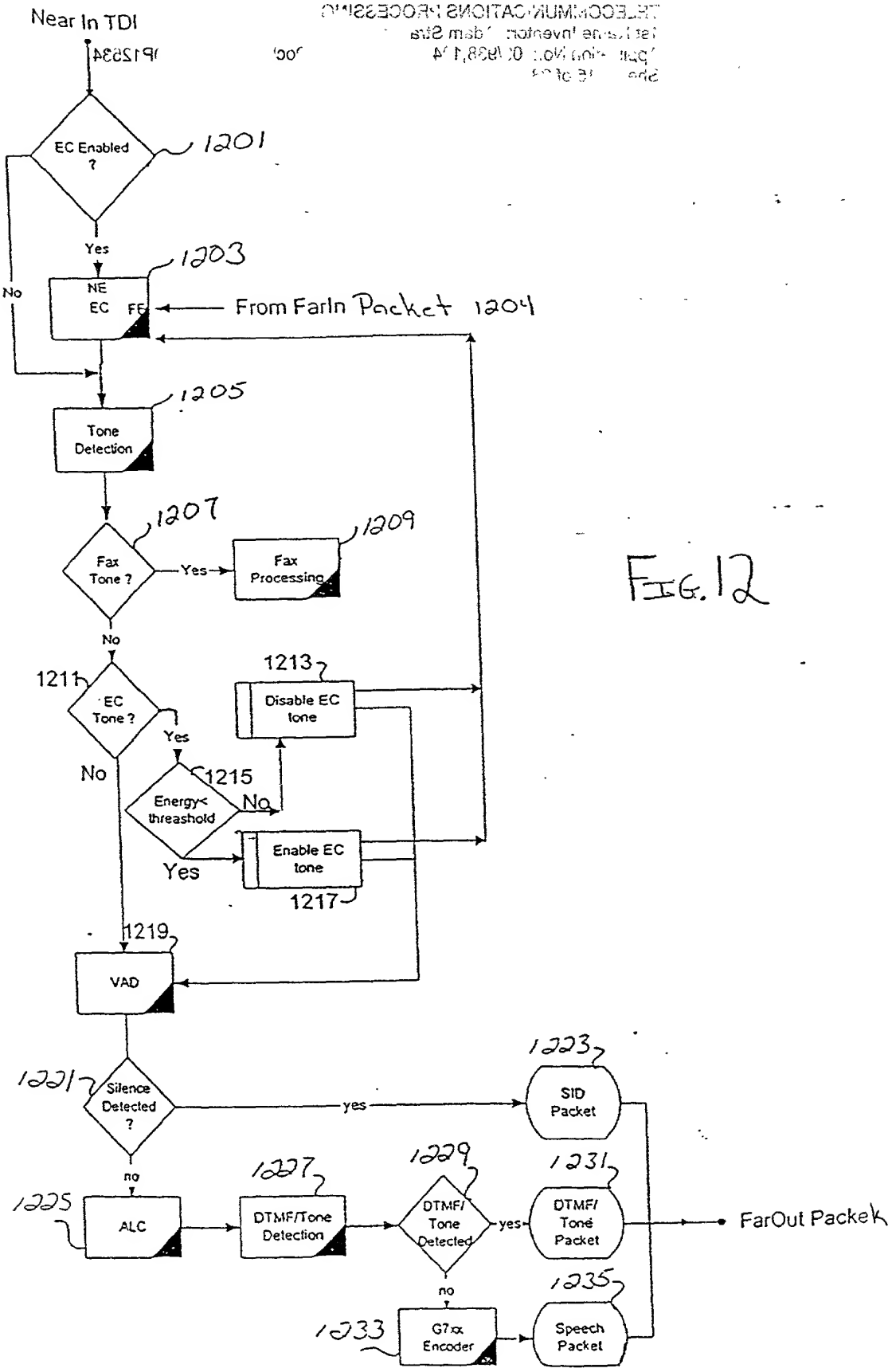

Near In TDI
EC Enabled ?
1201
Yes
No
1203
NE
EC FE
From FarIn Packet 1204
1205
Tone Detection
1207
Fax Tone ?
Yes
1209
Fax Processing
No
1211
EC Tone ?
Yes
No
1213
Disable EC tone
1215
Energy< threashold
No
Yes
Enable EC tone
1217
1219
VAD
1221
Silence Detected ?
yes
1223
SID Packet
no
1225
ALC
1227
DTMF/Tone Detection
1229
DTMF/ Tone Detected
yes
1231
DTMF/ Tone Packet
FarOut Packek
no
1233
G7xx Encoder
1235
Speech Packet

FIG. 12

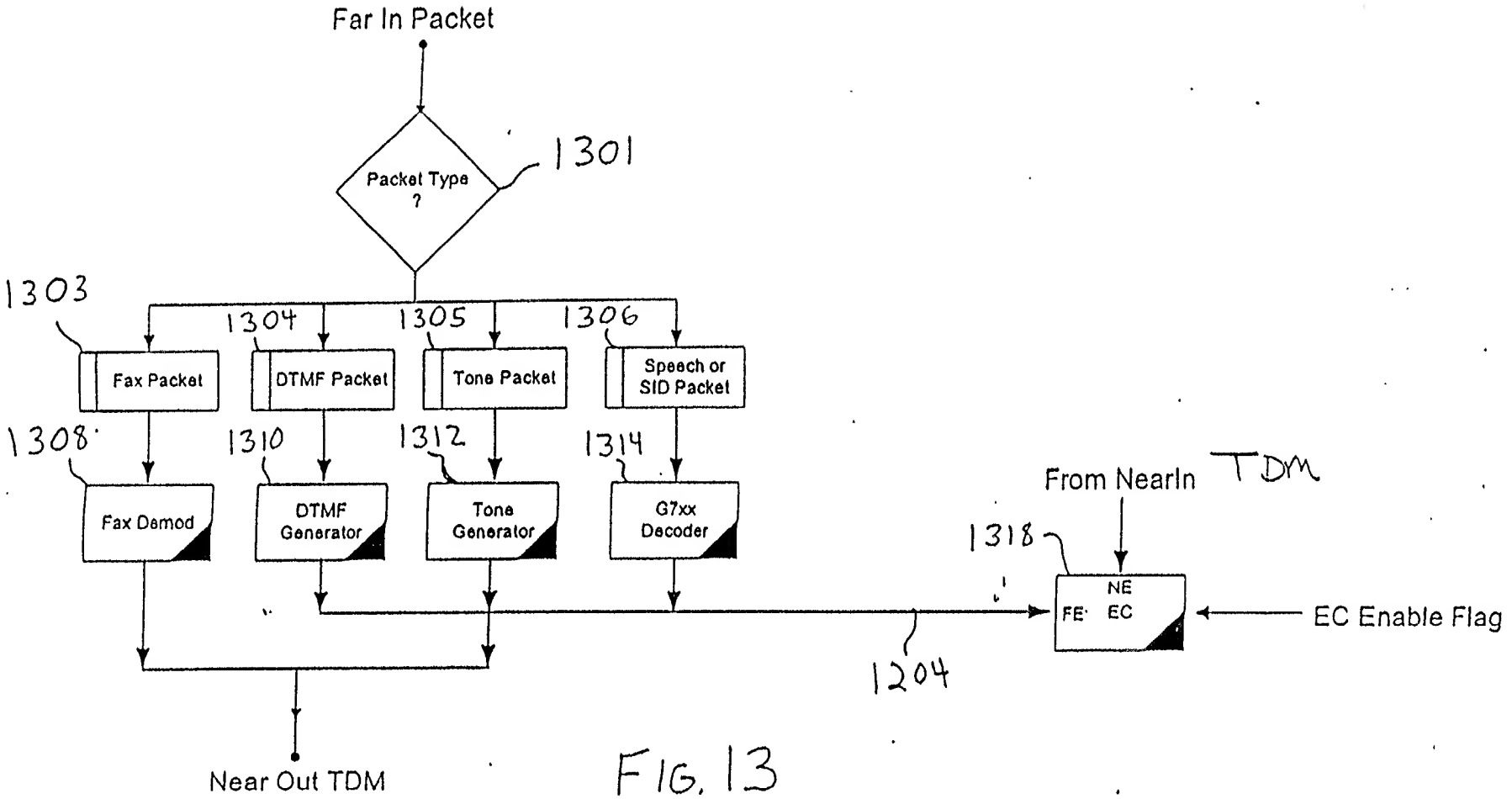

Far In Packet
Packet Type ?
1301
1303
1304
1305
1306
Fax Packet
DTMF Packet
Tone Packet
Speech or SID Packet
1308
1310
1312
1314
Fax Demod
DTMF Generator
Tone Generator
G7xx Decoder
From NearIn
TDM
1318
NE
FE
EC
EC Enable Flag
1204
Near Out TDM

FIG. 13

TOTE2T "HOTBE660

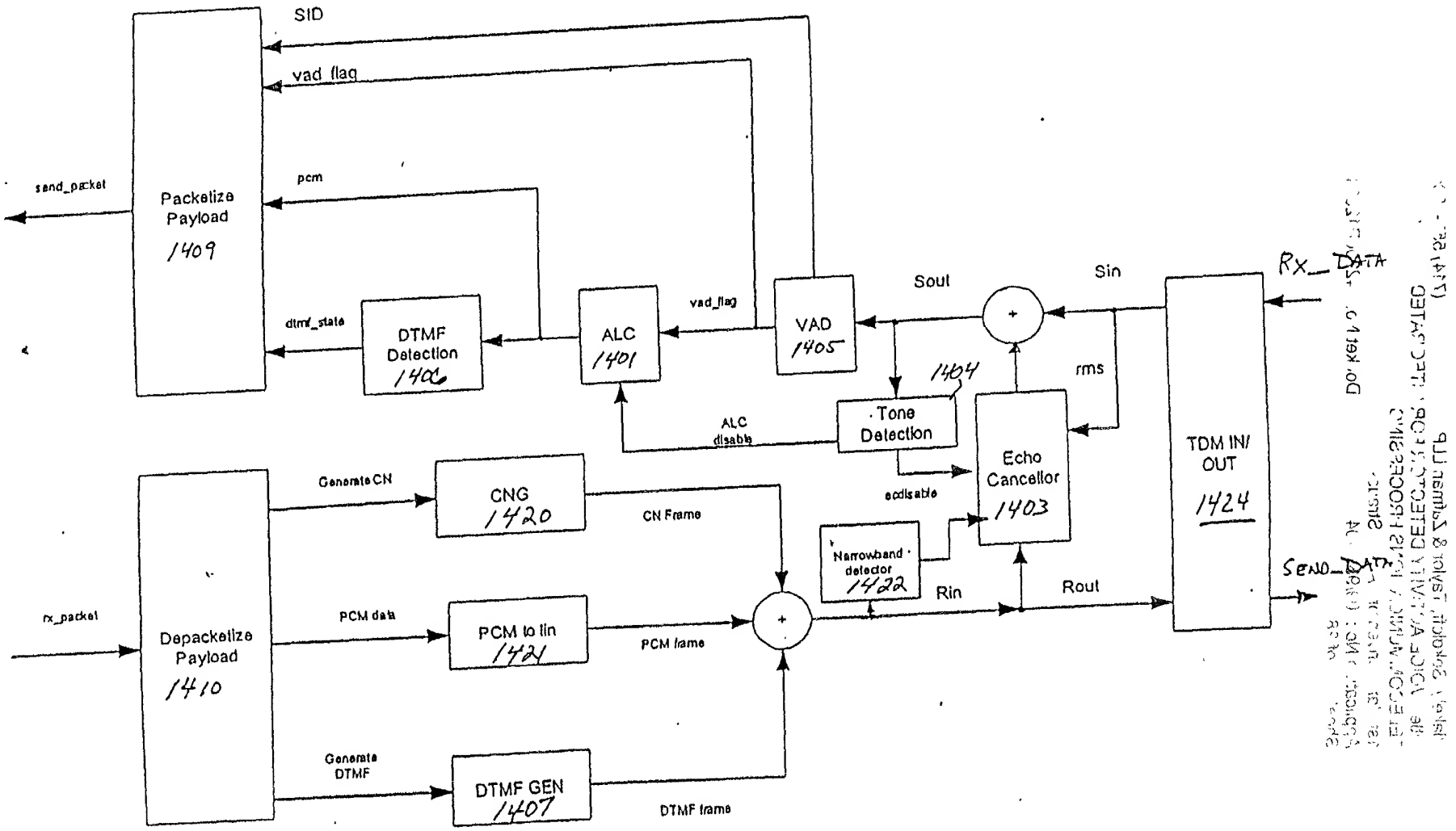


FIG. 14A

VxTel Voice Activity Detection Algorithm

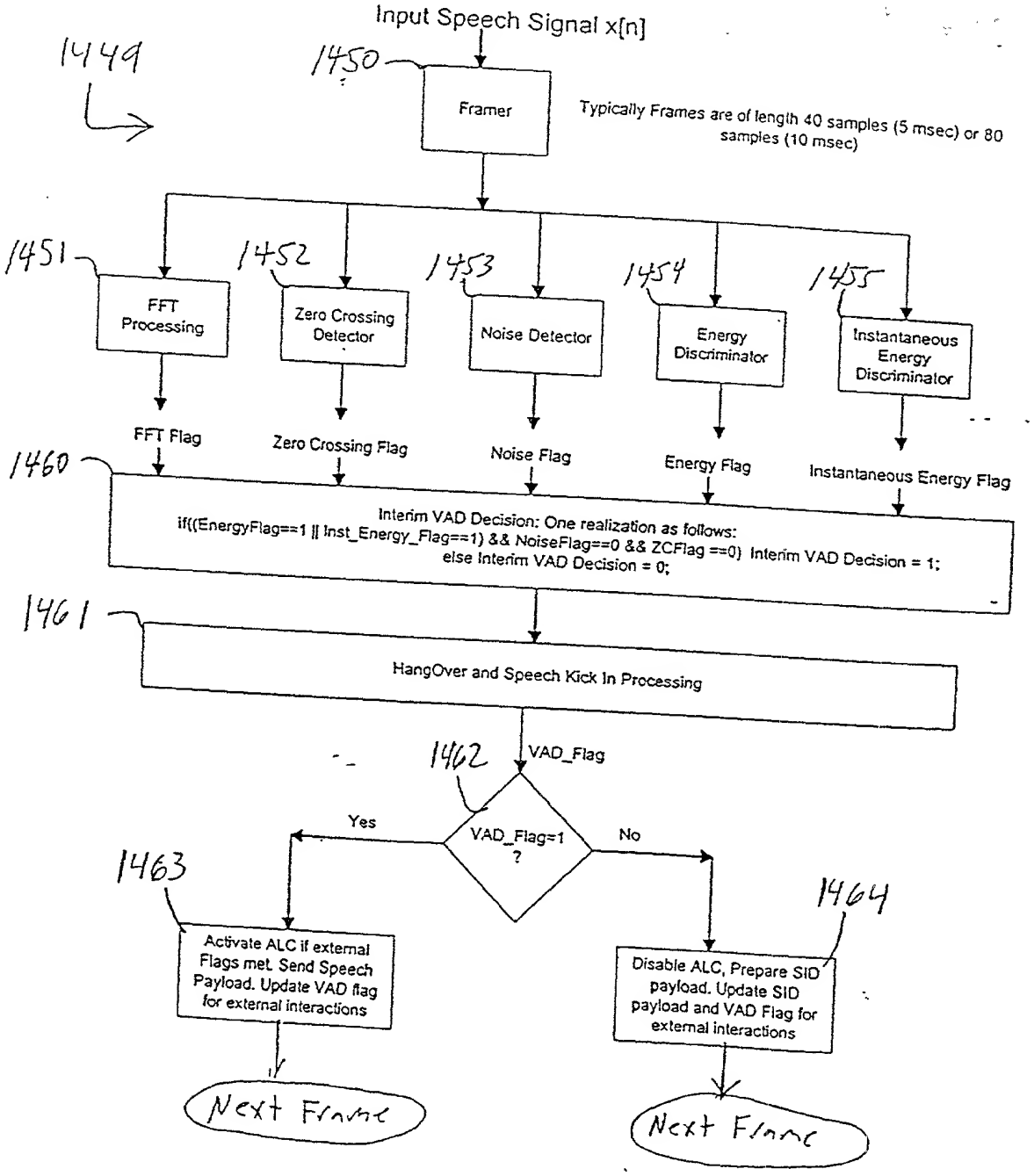


FIG. 14B

FFT Processing of Input Speech for VAD 1451

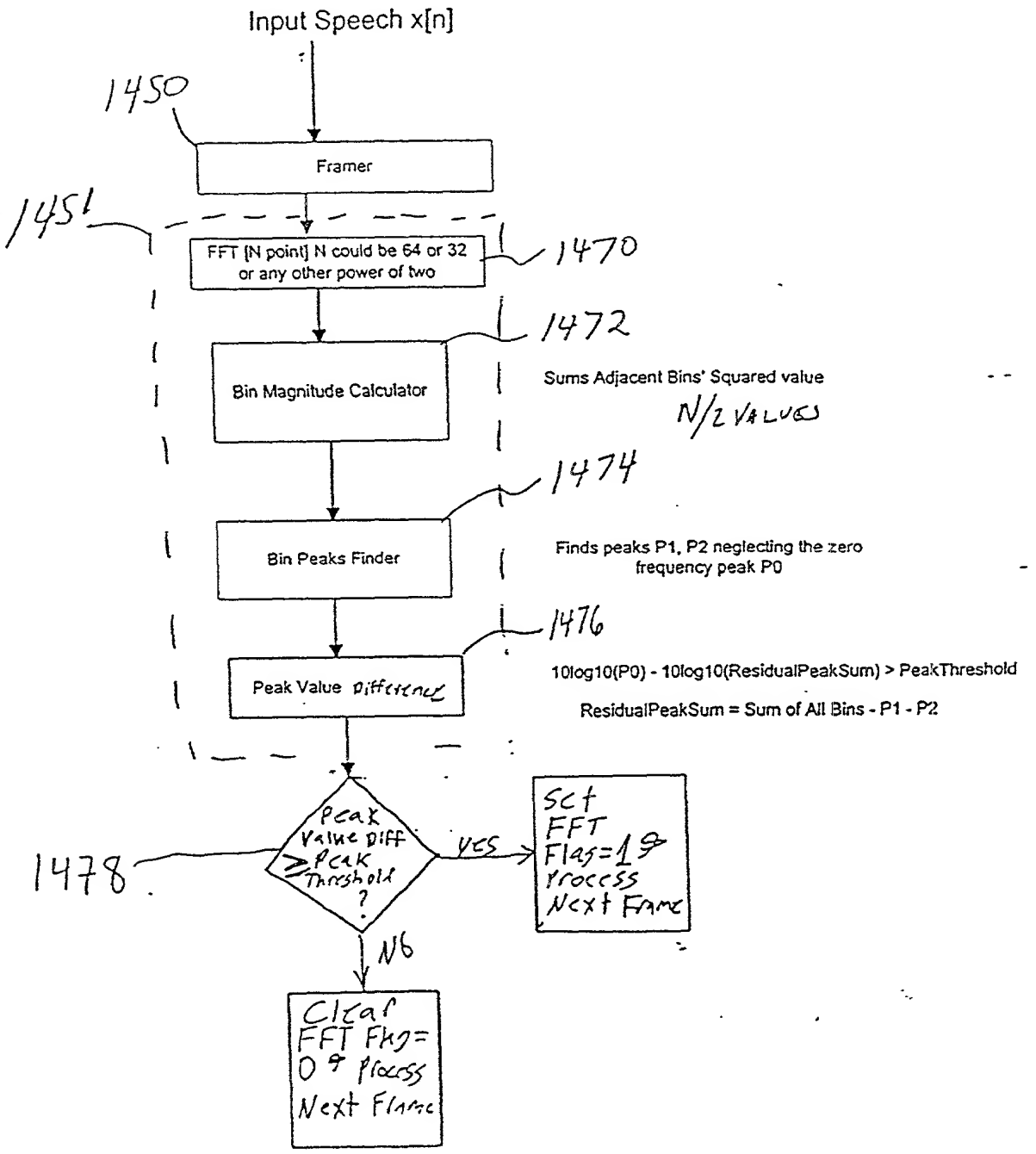


FIG. 14C

Blakely, Sokoloff, Taylor & Zafman LLP (714) 557-3800
Title: VOICE ACTIVITY DETECTOR INTEGRATED
TELECOMMUNICATIONS PROCESSING
Serial No. Inventor: Adam Sroubek
Application No. 09/[illegible]
Filed: [illegible]

Zero Crossing Detector 1452

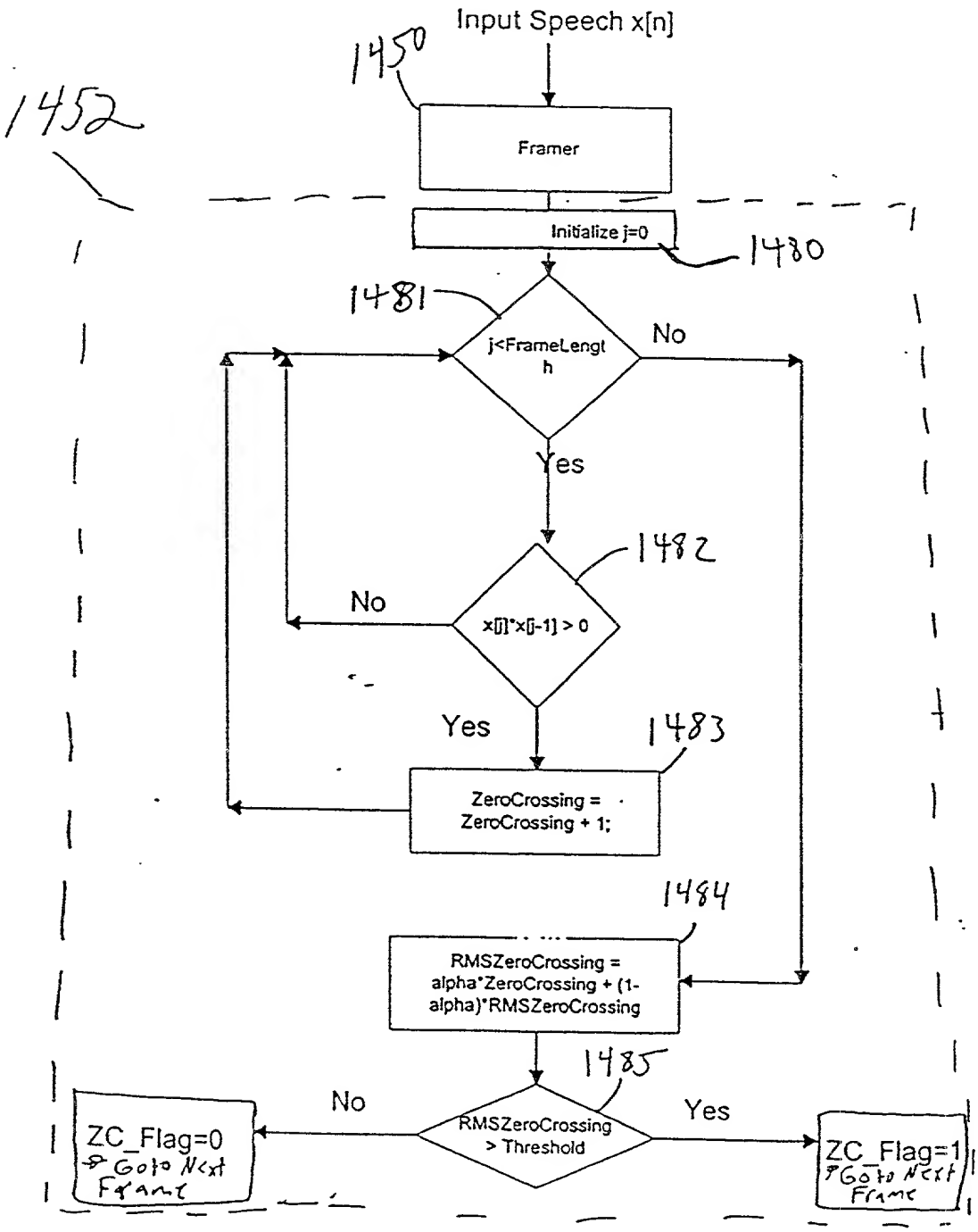


FIG. 14D

Noise Detection in VAD

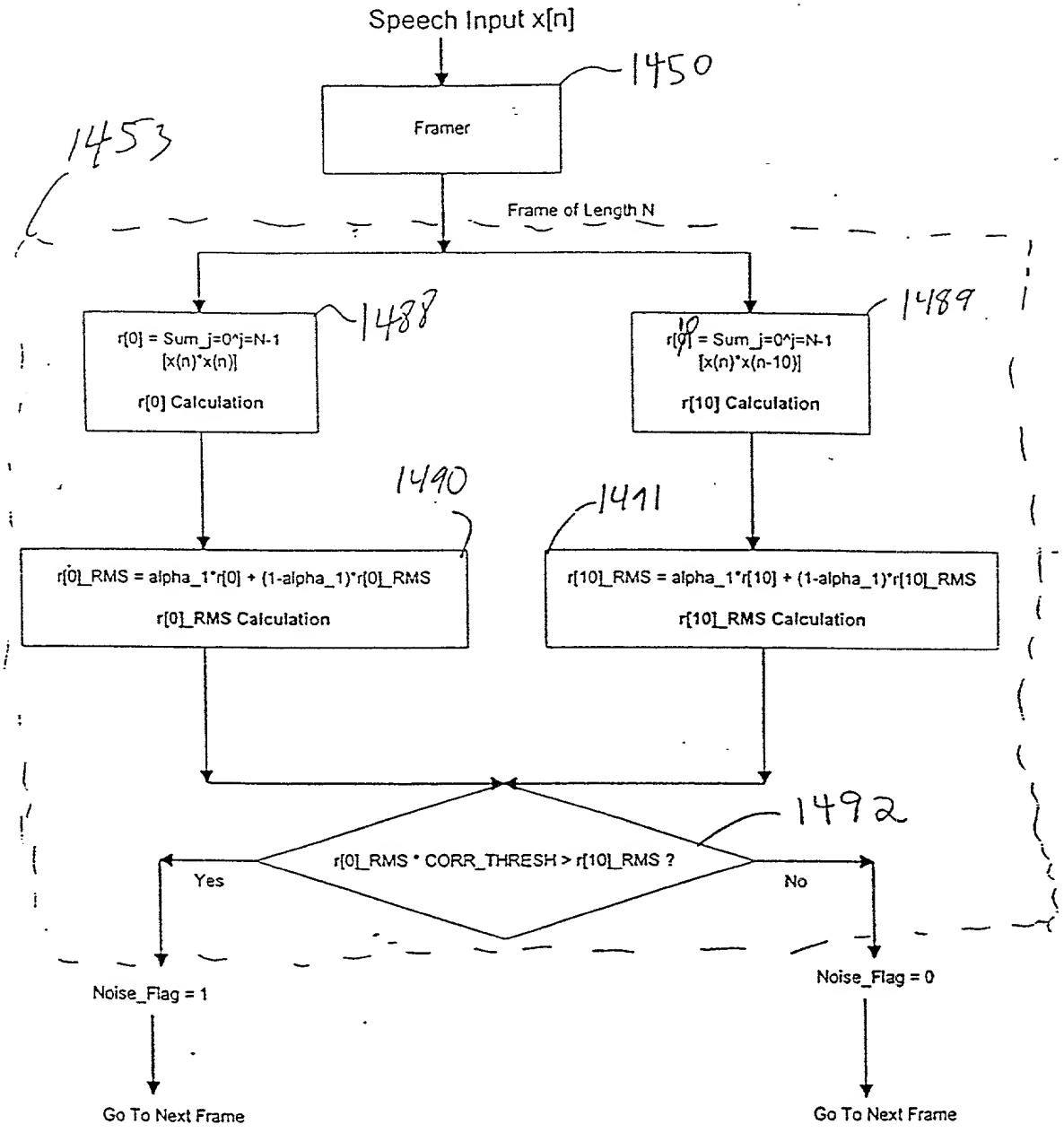


FIG. 14E

Energy Discriminator 1454

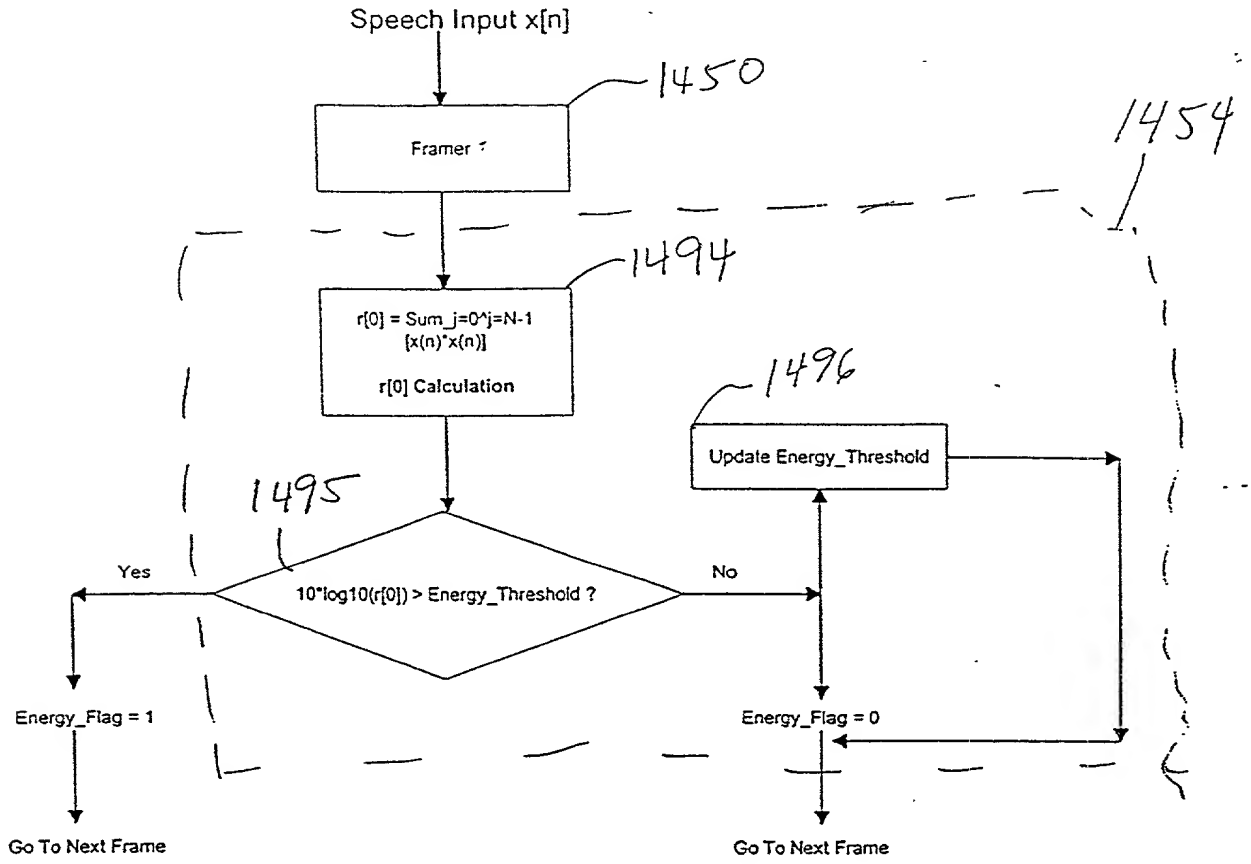


FIG. 14F

Blakely, Taylor & Zafman LLP (714) 85 -3800
VOICE ACTIVITY DETECTOR FOR INTEGRATED
TE ECOT TUNICATIONS PROCESSING
"s' Name Inventor: Adam Sussex
Application No : 09/239 104 Docket No.: 42390-1254

Instantaneous Energy Discriminator 1455

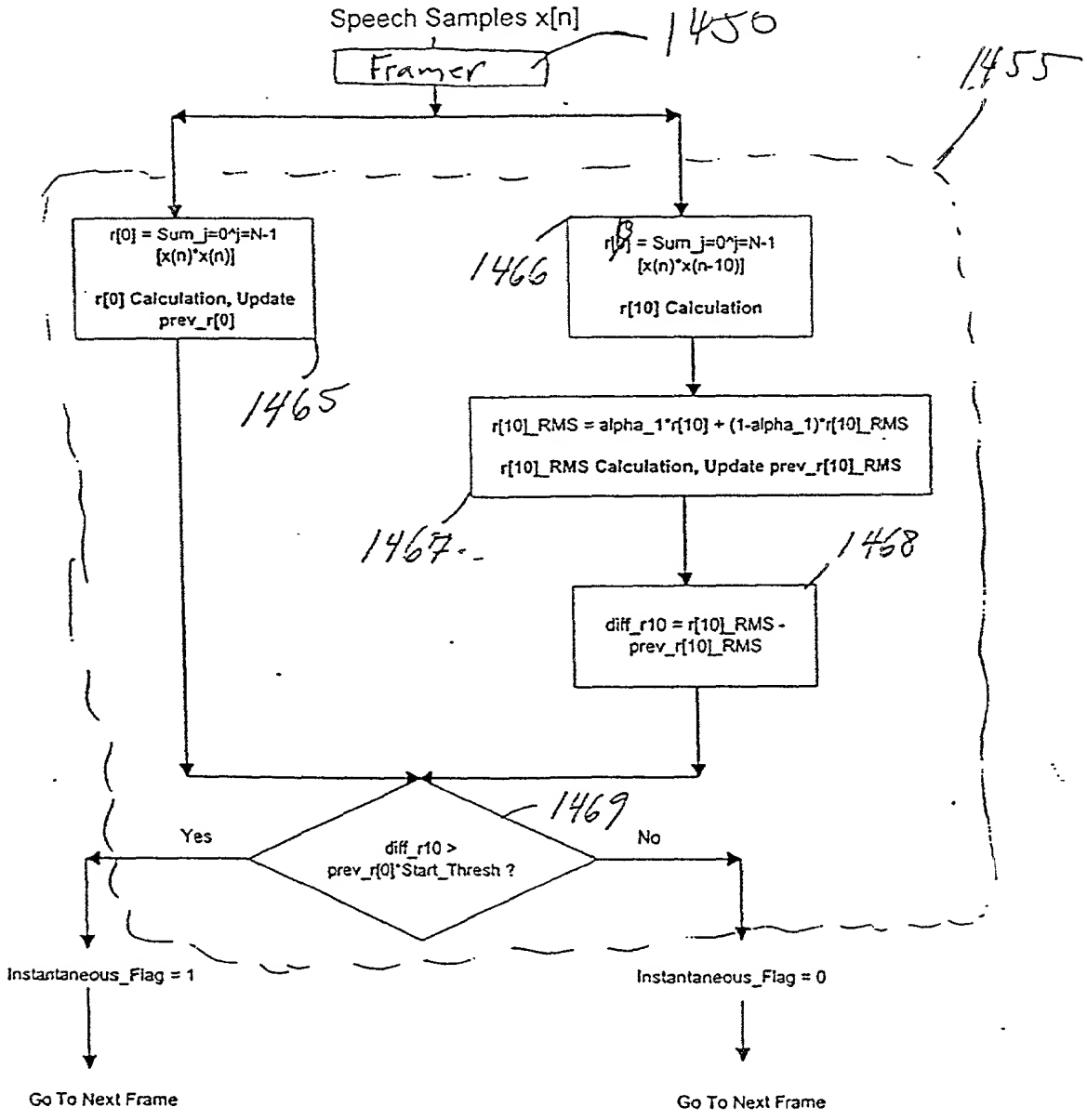


Fig. 14G

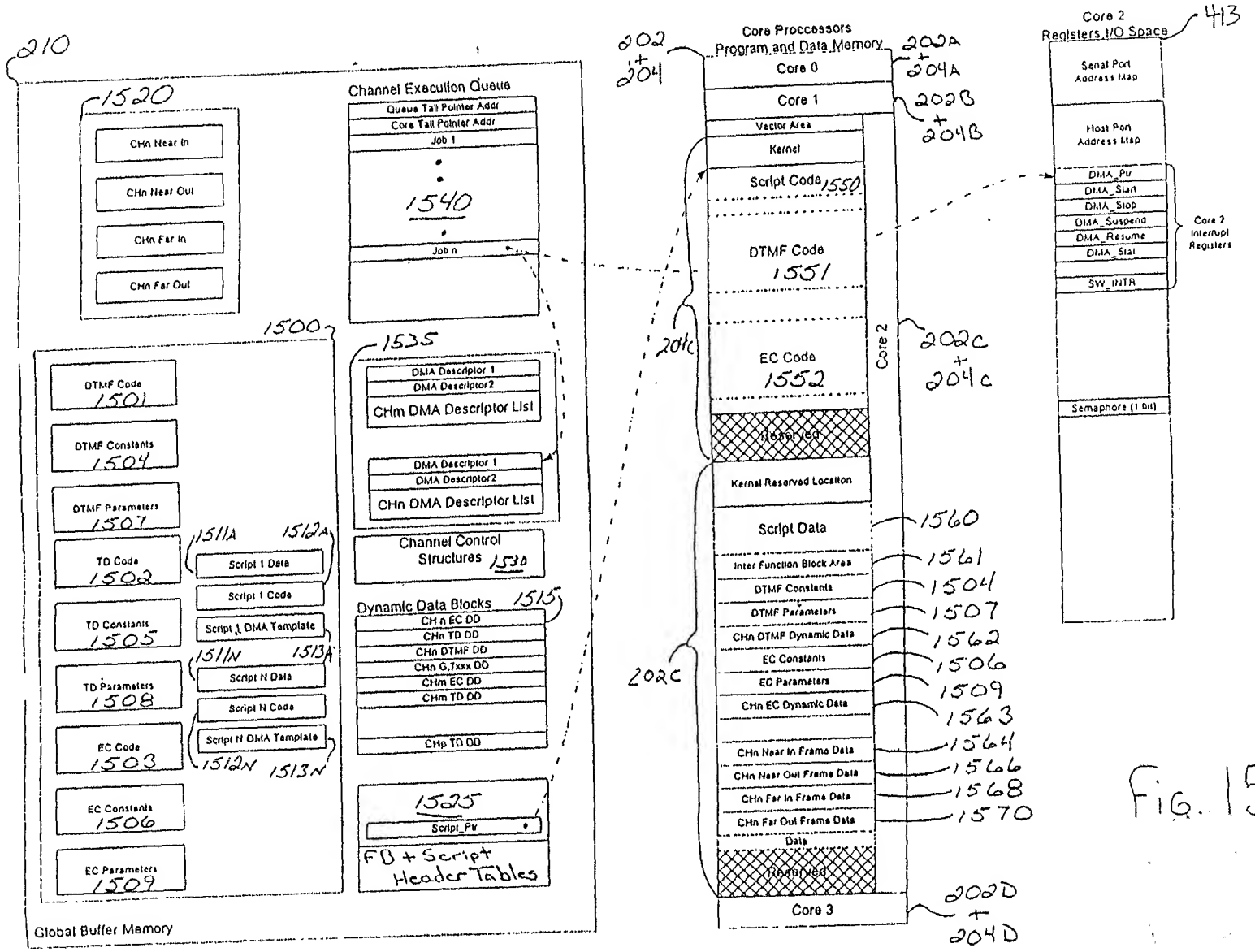

210
1520
CHn Near In
CHn Near Out
CHn Far In
CHn Far Out
Channel Execution Queue
Queue Tail Pointer Addr
Core Tail Pointer Addr
Job 1
1540
Job n
1500
1535
DTMF Code 1501
DTMF Constants 1504
DTMF Parameters 1507
TD Code 1502
TD Constants 1505
TD Parameters 1508
EC Code 1503
EC Constants 1506
EC Parameters 1509
1511A
1512A
Script 1 Data
Script 1 Code
Script 1 DMA Template
1511N
1513A
Script N Data
Script N Code
Script N DMA Template
1512N
1513N
DMA Descriptor 1
DMA Descriptor2
CHm DMA Descriptor List
DMA Descriptor 1
DMA Descriptor2
CHn DMA Descriptor List
Channel Control Structures 1530
Dynamic Data Blocks
1515
CHn EC DD
CHn TD DD
CHn DTMF DD
CHn G.7xxx DD
CHm EC DD
CHm TD DD
CHp TD DD
1525
Script_Ptr
FB + Script Header Tables
Global Buffer Memory
202 + 204
Core Processors Program and Data Memory
202A + 204A
Core 0
202B + 204B
Core 1
Vector Area
Kernel
Script Code 1550
DTMF Code 1551
204c
EC Code 1552
Core 2
202C + 204c
Reserved
Kernal Reserved Location
Script Data
1560
Inter Function Block Area
1561
DTMF Constants
1504
DTMF Parameters
1507
CHn DTMF Dynamic Data
1562
EC Constants
1506
EC Parameters
1509
CHn EC Dynamic Data
1563
CHn Near In Frame Data
1564
CHn Near Out Frame Data
1566
CHn Far In Frame Data
1568
CHn Far Out Frame Data
1570
Data
Reserved
202C
202D + 204D
Core 3
Core 2 Registers I/O Space
413
Serial Port Address Map
Host Port Address Map
DMA_Ptr
DMA_Start
DMA_Stop
DMA_Suspend
DMA_Resume
DMA_Stat
SW_INTR
Core 2 Interrupt Registers
Semaphore (1 bit)

Fig. 15

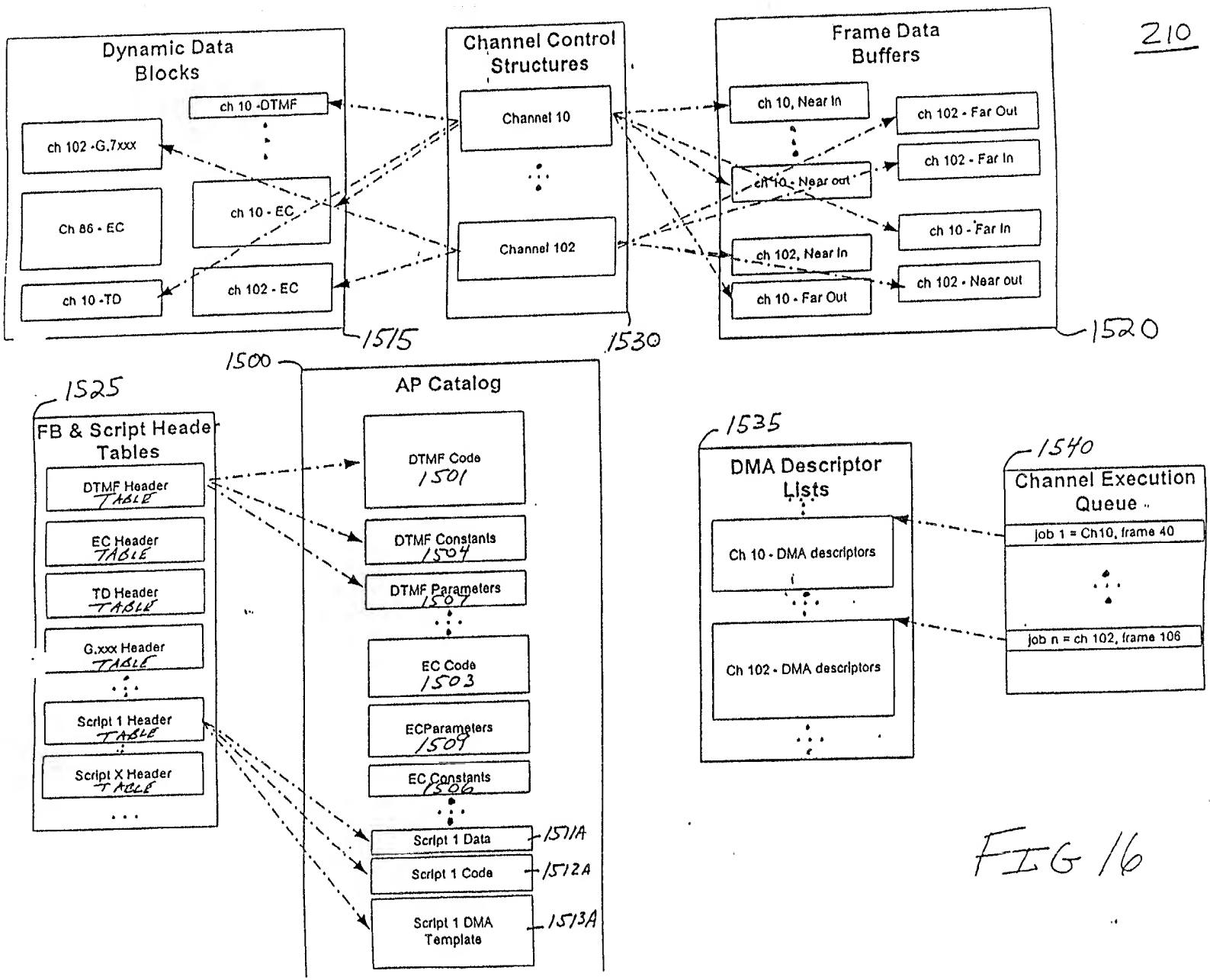

Dynamic Data Blocks
ch 10 -DTMF
ch 102 -G.7xxx
Ch 86 - EC
ch 10 - EC
ch 10 -TD
ch 102 - EC
1515
Channel Control Structures
Channel 10
Channel 102
1530
Frame Data Buffers
ch 10, Near In
ch 10 - Near out
ch 102, Near In
ch 10 - Far Out
ch 102 - Far Out
ch 102 - Far In
ch 10 - Far In
ch 102 - Near out
1520
210
1500
AP Catalog
1525
FB & Script Header Tables
DTMF Header TABLE
EC Header TABLE
TD Header TABLE
G.xxx Header TABLE
Script 1 Header TABLE
Script X Header TABLE
DTMF Code 1501
DTMF Constants 1504
DTMF Parameters 1507
EC Code 1503
ECParameters 1509
EC Constants 1506
Script 1 Data
Script 1 Code
Script 1 DMA Template
1571A
1512A
1513A
1535
DMA Descriptor Lists
Ch 10 - DMA descriptors
Ch 102 - DMA descriptors
1540
Channel Execution Queue
job 1 = Ch10, frame 40
job n = ch 102, frame 106

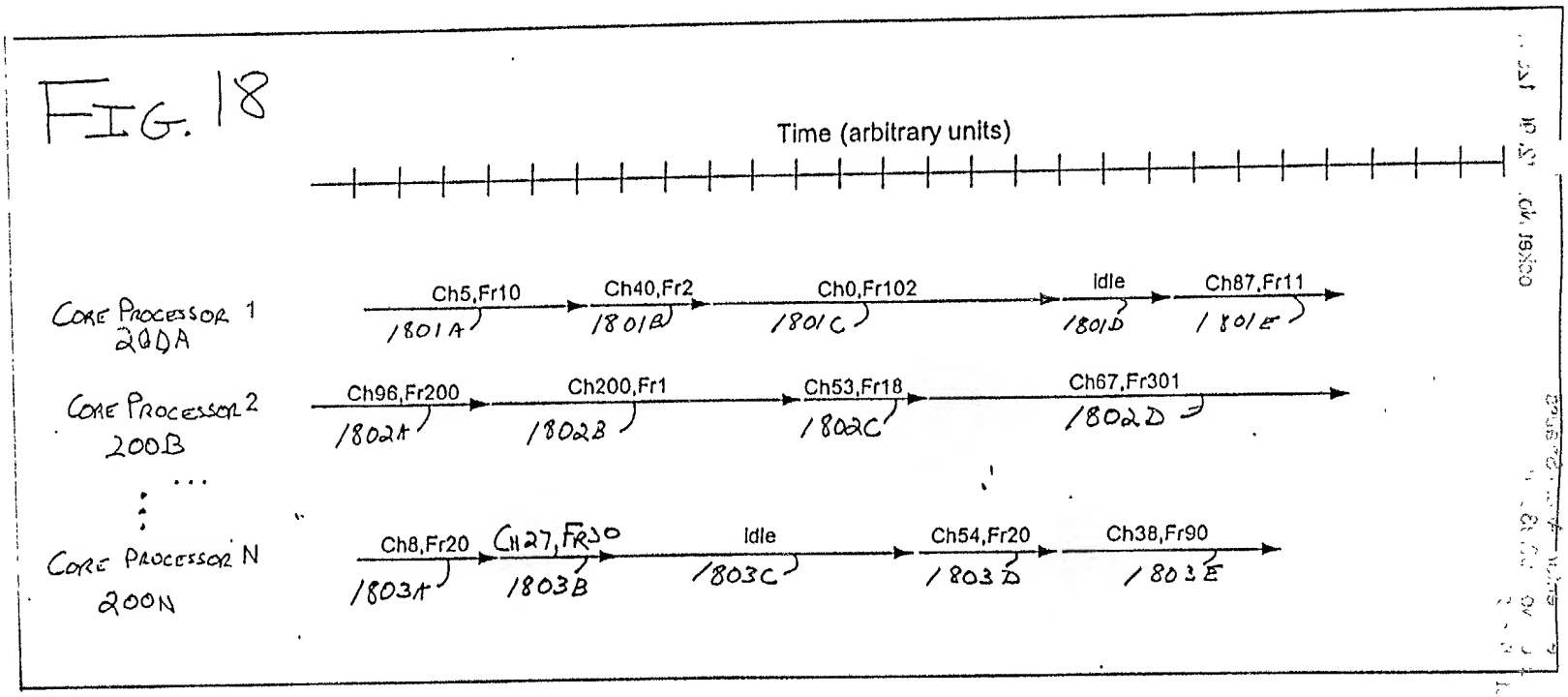
FIG 16

Blakely, Sokoloff, Taylor & Zafman LLP
Title: VOICE ACTIVITY DETECTOR FOR INTEGRATED
For: ECOMMUNICATIONS PROCESSING
Name Inventor: Adam Straus
Serial No.: 09/935,104

Fig. 1

09/935,104

FIG. 18


Time (arbitrary units)
Core Processor 1
200A
Ch5,Fr10
1801A
Ch40,Fr2
1801B
Ch0,Fr102
1801C
Idle
1801D
Ch87,Fr11
1801E
Core Processor 2
200B
Ch96,Fr200
1802A
Ch200,Fr1
1802B
Ch53,Fr18
1802C
Ch67,Fr301
1802D
Core Processor N
200N
Ch8,Fr20
1803A
Ch27,Fr30
1803B
Idle
1803C
Ch54,Fr20
1803D
Ch38,Fr90
1803E